

**AMENDMENTS TO THE CLAIMS**

1. (Original) An active matrix display device having a plurality of thin film transistors disposed in a matrix on an insulating substrate and wiring connected to these thin film transistors;

wherein said active matrix display device comprises a flattening layer surrounding said wiring, and

a surface of said wiring and a surface of said flattening layer form substantially the same plane.

2. (Original) The active matrix display device according to claim 1;  
wherein said wiring includes gate wiring, source wiring, and drain wiring,  
said gate wiring constituting scanning lines connected to gate electrodes of said thin film transistors,

said source wiring and said drain wiring being respectively connected to source electrodes and drain electrodes of said thin film transistors,

one of said source wiring and said drain wiring constituting signal lines adapted to supply signals to said thin film transistors while the other is connected to pixel electrodes,

and wherein said flattening layer surrounds said source electrodes, said drain electrodes, said source wiring, and said drain wiring,

surfaces of said source electrodes, said drain electrodes, said source wiring, and said drain wiring, and the surface of said flattening layer forming substantially the same plane.

3. (Currently Amended) The active matrix display device according to ~~claim 1 or 2~~ claim 1, wherein said flattening layer is formed of a resin.

4. (Original) The active matrix display device according to claim 3, wherein said flattening layer is formed of a photosensitive resin composition.

5. (Original) The active matrix display device according to claim 1, wherein said flattening layer comprises an inorganic substance.

6. (Original) The active matrix display device according to claim 1, wherein said flattening layer is formed by the use of a resin composition comprising an alkali-soluble alicyclic olefin resin and a radiation sensitive component.

7. (Original) The active matrix display device according to claim 1, wherein said source electrodes, said drain electrodes, said source wiring, and said drain wiring each contain an organic substance.

8. (Original) The active matrix display device according to claim 1, wherein said insulating substrate is formed of a transparent material.

9. (Original) The active matrix display device according to claim 1, wherein said insulating substrate is a substrate having a surface covered with an insulator.

10. (Original) The active matrix display device according to claim 1, wherein said display device is a liquid crystal display device.

11. (Original) The active matrix display device according to claim 1, wherein said display device is an organic EL display device.

12. (Original) A manufacturing method of an active matrix display device comprising:  
a step of forming a gate electrode and gate wiring on an insulating substrate;  
a step of forming an insulating film so as to cover said gate electrode and said gate wiring;  
a step of selectively forming a semiconductor layer on said insulating film;  
a step of forming a flattening layer on said semiconductor layer;  
a step of selectively removing part of said flattening layer to form a groove reaching said semiconductor layer; and  
a step of forming a wiring portion in said groove such that a surface of said wiring portion and a surface of said flattening layer form substantially the same plane, said wiring portion reaching said semiconductor layer.

13. (Original) The manufacturing method of an active matrix display device according to claim 12, wherein said step of forming said wiring portion includes:  
a step of forming a wiring formation assisting layer; and

a step of filling said groove with a wiring material.

14. (Original) The manufacturing method of an active matrix display device according to claim 13, wherein said wiring formation assisting layer is one of a liftoff layer, a catalyst layer, and a water repellent layer.

15. (Original) The manufacturing method of an active matrix display device according to claim 13, wherein said flattening layer serves as said wiring formation assisting layer.

16. (Original) The manufacturing method of an active matrix display device according to claim 12, wherein said step of selectively forming said semiconductor layer includes:

a step of forming a layer of a first semiconductor;

a step of stacking, on said layer of said first semiconductor, a layer of a second semiconductor having a conductivity different from that of said first semiconductor;

a step of stacking a photoresist on a stacked film of said first semiconductor and said second semiconductor;

a step of removing by an entire thickness a portion, other than on a predetermined element region, of said photoresist and by part of a thickness a portion, on a channel region in said element region, of said photoresist;

a step of, using the remainder of said photoresist as a mask, selectively removing a portion, other than said element region, of said stacked film of said first and second semiconductors and said layer of said second semiconductor on said channel region; and

a step of selectively forming a protective film on said channel region of said layer of said first semiconductor.

17. (Original) The manufacturing method of an active matrix display device according to claim 16, wherein said step of removing said photoresist includes:

a step of exposing said photoresist by adjusting an exposure amount so that a remaining thickness of said photoresist on said channel region becomes thinner as compared with a remaining thickness of said photoresist on the other portion of the element region; and

a step of developing the exposed photoresist to remove the photoresist on a portion other than said element region, thereby obtaining a patterned photoresist;

and wherein in said step of forming said protective film, a portion of said patterned photoresist remaining through said semiconductor selectively removing step is used as a mask.

18. (Original) The manufacturing method of an active matrix display device according to claim 16, wherein said step of forming said protective film includes a step of directly nitriding the surface of said channel region.

19. (Original) The manufacturing method of an active matrix display device according to claim 13, wherein said step of filling said groove with said wiring material is carried out by one of a sputtering method, a CVD method, a plating method, and a printing method.

20. (Original) The manufacturing method of an active matrix display device according to claim 19, wherein said printing method is an inkjet printing method or a screen printing method.

21. (Currently Amended) The manufacturing method of an active matrix display device according to ~~any of claims 12 to 20~~ claim 12, wherein said display device is a liquid crystal display device.

22. (Currently Amended) The manufacturing method of an active matrix display device according to ~~any of claims 12 to 20~~ claim 12, wherein said display device is an organic EL display device.

23. (Original) A thin film transistor integrated circuit device having a plurality of thin film transistors formed on an insulating substrate and wiring connected to these thin film transistors, wherein said thin film transistor integrated circuit device comprises a flattening layer surrounding said wiring, and a surface of said wiring and a surface of said flattening layer form substantially the same plane.

24. (Original) The thin film transistor integrated circuit device according to claim 23; wherein said wiring includes gate wiring, source wiring, and drain wiring, said gate wiring being connected to a gate electrode of at least one of said thin film transistors;

said source wiring being connected to a source electrode of at least one of said thin film transistors; and

said drain wiring being connected to a drain electrode of at least one of said thin film transistors;

and wherein said flattening layer surrounds said source electrode, said drain electrode, said source wiring, and said drain wiring;

surfaces of said source electrode, said drain electrode, said source wiring, and said drain wiring, and the surface of said flattening layer forming substantially the same plane.

25. (Original) The thin film transistor integrated circuit device according to claim 24, wherein an insulating film is provided so as to surround said gate electrodes of said thin film transistors and said gate wiring;

said gate electrodes of said thin film transistors, said gate wiring, and said insulating film forming substantially the same flat surface, and

a gate insulating film of said thin film transistors is formed on said flat surface.

26. (Original) A manufacturing method of a thin film transistor integrated circuit device, comprising:

a step of forming gate electrodes and a gate wiring on an insulating substrate;

a step of forming an insulating film so as to cover said gate electrodes and said gate wiring,

a step of selectively forming a semiconductor layer on said insulating film;

a step of forming a flattening layer on said semiconductor layer;

a step of selectively removing part of said flattening layer to form a groove reaching said semiconductor layer; and

a step of forming a wiring portion in said groove such that a surface of said wiring portion and a surface of said flattening layer form substantially the same plane, said wiring portion reaching said semiconductor layer.

27. (Original) The manufacturing method of a thin film transistor integrated circuit device according to claim 26, wherein said step of forming said wiring portion includes:

a step of forming a wiring formation assisting layer; and

a step of filling said groove with a wiring material.

28. (Original) The manufacturing method of a thin film transistor integrated circuit device according to claim 27, wherein said wiring formation assisting layer is one of a liftoff layer, a catalyst layer, and a water repellent layer.

29. (Original) The manufacturing method of a thin film transistor integrated circuit device according to claim 27, wherein said flattening layer serves as said wiring formation assisting layer.

30. (Original) The manufacturing method of a thin film transistor integrated circuit device according to claim 26, wherein said step of selectively forming said semiconductor layer includes:

a step of forming a layer of a first semiconductor;

a step of stacking, on said layer of said first semiconductor, a layer of a second semiconductor having a conductivity different from that of said first semiconductor;

a step of stacking a photoresist on a stacked film of said first semiconductor and said second semiconductor;

a step of removing by an entire thickness a portion, other than on a predetermined element region, of said photoresist and by part of a thickness a portion, on a channel region in said element region, of said photoresist;

a step of, using the remainder of said photoresist as a mask, selectively removing a portion, other than said element region, of said stacked film of said first and second semiconductors and said layer of said second semiconductor on said channel region; and

a step of selectively forming a protective film on said channel region of said layer of said first semiconductor.

31. (Original) The manufacturing method of a thin film transistor integrated circuit device according to claim 30, wherein said step of removing said photoresist includes:

a step of exposing said photoresist by adjusting an exposure amount so that a remaining thickness of said photoresist on said channel region becomes thinner as compared with a remaining thickness of said photoresist on the other portion of the element region; and

a step of developing the exposed photoresist to remove the photoresist on a portion other than said element region, thereby obtaining a patterned photoresist;

and wherein in said step of forming said protective film, a portion of said patterned photoresist remaining through said semiconductor selectively removing step is used as a mask.